REMARKS

Present Status of the Application

The Office Action rejected claims 1-6, 8, 9 and 35-37 under 35 U.S.C. 102(b), as being anticipated by Yang (U.S. 6,093,945). The Office Action also rejected claims 1, 7, 10 and 12 under 35 U.S.C. 102(b) as being anticipated by Liang et al. (U.S. 5,714,412; hereafter Liang). The Office Action rejected claim 11 under 35 U.S.C. 103(a), as being unpatentable over Yang as applied to claim 1 above and further in view of Schwabe et al. (U.S. 4,257,832; hereafter Schwabe). Applicants have amended claims 1, 4, 8 and 35 can cancel claims 2-3 and 7 to improve clarity. After entry of the foregoing amendments, claims 1, 4-6, 8-12 and 35-37 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

The Office Action rejected claims 1-6, 8, 9 and 35-37 under 35 U.S.C. 102(b), as being anticipated by Yang (U.S. 6,093,945). The Office Action also rejected claims 1, 7, 10 and 12 under 35 U.S.C. 102(b) as being anticipated by Liang et al. (U.S. 5,714,412; hereafter Liang) and asserted that Yang and Liang disclose all claimed features of the present invention.

Applicants respectfully traverse the rejections but have amended chaims 1 and 35 by adding the claimed features of claims 2-3 and 7 for further clarity. No new matter has

been introduced into the application by the amendment made herein. Furthermore, for at least the reasons set forth below, Applicants respectfully submit that the amended claims 1 and 35 patentably distinguish over the cited arts.

It is well established that anticipation under 35 U.S.C. 102 requires each and every elements of the rejected claims must be disclosed exactly by a single prior art reference.

The amended independent claims 1 and 35 are allowable for at least the reason that Yang and Liang fail to teach or disclose each and every features of the proposed amended independent claims 1 and 35. As amended, claims 1 and 35 recite respectively:

> Claim 1. A split-gate non-volatile memory cell, comprising:
> a substrate;
> a charge-trapping layer on the substrate;
> a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer, wherein the split gate is composed of at least two separated conductive pieces and **the conductive pieces are electrically connected to a common voltage source**; and
> a source/drain in the substrate beside the split gate, wherein
> the charge-trapping layer around the split region serves as a coding region.
>
> Claim 35. An operating method of a split-gate non-volatile memory cell, wherein
> the split-gate non-volatile memory cell comprises:
> a substrate;
> a charge-trapping layer on the substrate;
> a split gate on the charge-trapping layer, including at least one split region directly over the charge-trapping layer, wherein the charge-trapping layer around the split region serves as a coding region, the split gate is composed of at least two separated conductive pieces and **the conductive pieces are electrically connected to a common voltage source**; and
> a source/drain in the substrate beside the split gate, and
> the operating method comprises:
> in a programming operation:
> applying 0V to the substrate and the source/drain; and
> applying a first negative voltage to the split gate, the first negative voltage being sufficiently high for injecting electrons into the coding region;

and

in an erasing operation:

applying 0V to the split gate, wherein **each conductive piece is at an electric state of 0 V**;

floating the source/drain; and

applying a second negative voltage to the substrate, the second positive voltage being sufficiently high for ejecting electrons from the coding region.

(***Emphasis added***). Applicants submit that claims 1 and 35 patently define over the cited arts for at least the reason that the cited art fails to disclose at least the features emphasized above.

More specifically, both Yang and Liang fail to teach or suggest that the conductive pieces of the split gate is electrically connected to a common source voltage. In the present invention, the linear conductive spacers 330 are directly connected with the boundary conductor 338 and the linear conductor 340 separated from the linear conductive spacers 330 and the boundary conductor 338 by the dielectric layer 333 is electrically connected to an operating line 390 via a contact 380 (paragraph [0035] and Fig. 4 of the present invention). That is, the linear conductive spacers 330 and the linear conductor 340 are connected to the same voltage source.

However, in the cited art, Yang provide a flash memory cell with a pair of spacer-shaped floating gates 14 and a control gate 19 located over the floating gates 14 and separated from the floating gates 14 by a inter-poly dielectric layer. It is well known in the art that in the flash memory, the floating gate is electrically isolated from the voltage source or the external electrode such as control gate (col. 8, lines 1-37). Yang fails to suggest or teach that the floating gates 14 are electrically connected to the control

gate 19. Obviously, in Yang's application, by properly controlling the voltage applied on the control gate, the electrons or holes are punching through the tunnel oxide layer 13 and stored in the floating gates 14. More specifically, the floating gates 14 are served as the storage elements. Furthermore, Yang never mentions that the tunnel oxide layer 13 is used as the storage element instead of the floating gates. Therefore, people skilled in the art would not modify Yang's application by electrically connecting the control gate 19 and the floating gates 14 since there is no motivation founded in the cited art or suggested by Yang.

Furthermore, the Office Action asserted that Fig. 9C of Liang's application shows that different pieces of the split gate are electrically connected to each other. Nevertheless, Applicants respectfully disagree with this assertion. Applicants would like to attract Examiner's attention to Fig. 9A and Fig. 9C of Liang's application. Liang emphasizes that FG1 and FG2 are floating gates and are separated from the control gate CG by a silicon dioxide layer, wherein control gate CG is connected voltage V_G through a line to contact X3 (col. 6, lines 7-15). Liang further emphasizes that "the split gate structure of Fig. 9A provides the equivalent of two stacked gate FET transistors and an isolation FET transistor" (col. 6, lines 16-18). That is, as shown in Fig. 9A, both side portions of the split gate structure are stacked gate FET transistors comprising stacking control gate CG and floating gate FG1/FG2 and the central portion of the split gate structure is the isolation FET transistor with only one control gate CG. From the equivalent circuit point of view, it in undoubted that all the control gate GC of the stacked gate FET transistors and the isolation FET transistor are electrically connected to each

other. In Fig. 9C of Liang's application, it is clearly that the floating gates FG1 and FG2 of the stacked gate FET transistors are electrically isolated from the control gates.

In addition, Liang fails to teach or suggest that the floating gates FG1 and FG2 can be electrically connected to the control gate CG. Hence, people skilled in the art would not modify Liang's application by electrically connecting the control gate CG and the floating gates FG1 and FG2 since there is no motivation founded in the cited art or suggested by Liang.

Therefore, Yang and Liang substantially fail to teach each and every feature of claims 1 and 35, and therefore, both Yang and Liang cannot possibly anticipate the claimed invention as claimed in the proposed independent claims 1 and 35 in this regard.

Claims 4-6, 8-10, 12 and 36-37, which depend from claims 1 and 35 respectively, are also patentable over Yang and Liang, at least because of their dependency from an allowable base claim.

For at least the foregoing reasons, Applicants respectfully submit that claims 1, 4-6, 8-10, 12 and 36-37 patently define over Yang and Liang respectively, and therefore should be allowed. Reconsideration and withdrawal of the above rejections is respectfully requested.

The Office Action rejected claim 11 under 35 U.S.C. 103(a), as being unpatentable over Yang as applied to claim 1 above and further in view of Schwabe et al. (U.S. 4,257,832; hereafter Schwabe).

Since claim 11 is dependent claim which further define the invention recited in

claim 1, Applicants respectfully assert that these claims also are in condition for allowance according to the same reasons as discussed above for the rejection 102. Thus, reconsideration and withdrawal of this rejection are respectively requested.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1, 4-6, 8-12 and 35-37 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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